REMARKS

The Specification has been amended to correct grammatical errors. In addition, claims 1-3, 5, 9, 10, 12-19, 23, and 25 have been amended, and claim 11 has been cancelled. Therefore, claims 1-10 and 12-25 are currently pending in the case. Further examination and reconsideration of the presently claimed application are respectfully requested.

Section 102 Rejections:

Claims 1-4, 6-15, 17-19, and 21-24 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,410,403 to Wu (hereinafter referred to as "Wu"). Claim 11 has been canceled thereby rendering rejection of claim 11 moot. As will be set forth in more detail below, the § 102 rejections of claims 1-4, 6-10, 12-15, 17-19, and 21-24 are respectfully traversed.

The standard for "anticipation" is one of fairly strict identity. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. Of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987), MPEP 2131. None of the cited art teaches or suggests all limitations of the currently pending claims, some distinctive limitations of which are set forth in more detail below.

The cited art does not teach polishing an upper layer of a semiconductor topography to expose a first underlying layer, which is formed upon and in contact with a second underlying layer, etching away remaining portions of the first underlying layer to expose the second underlying layer, and subsequently planarizing the topography, which includes polishing the second underlying layer. Amended independent claim 1 recites, in part:

> polishing an upper layer of the semiconductor topography to expose a first underlying layer; etching away remaining portions of said first underlying layer to expose a second underlying layer, wherein the first underlying layer is formed upon and in contact with the second underlying layer; and subsequently planarizing the topography, wherein said planarizing comprises polishing the second underlying layer.

Amended independent claim 10 recites similar limitations. Support for the amendments to claims 1 and 10 may be found in the Specification, for example, on page 12, lines 20-21, page 16, lines 4-5, page 17, lines 11-16, and page 17, line 23 - page 18, line 9.

Wu discloses a method for planarizing a shallow trench isolation. Wu, however, does not disclose polishing an upper layer of a semiconductor topography to expose a first underlying layer, which is formed upon and in contact with a second underlying layer, etching away remaining portions of the first underlying layer to expose the second underlying layer, and subsequently planarizing the topography, which includes polishing the second underlying layer. For example, Wu states that "we sequentially form a pad oxide layer 14, a first nitride layer 18, a sacrificial oxide layer 22 and a second nitride layer 24 over a substrate 10." (Wu -- col. 2, lines 65-67.) As shown in Fig. 1 of Wu, second nitride layer 24 is the uppermost layer of the stack, and second nitride layer 24 is formed upon and in contact with sacrificial oxide layer 22. Wu also states that "we deposit an isolation oxide layer 34 (e.g., STI oxide) filling the trench 30 and over the second nitride layer 24." (Wu -- col. 3, lines 40-42.)

Wu further states that "we chemical-mechanical polish the oxide layer 34A and the second nitride layer 24A down to a level so that the second nitride layer 24A has a thickness of between about 50 and 200 Å." (Wu -- col. 3, lines 50-53.) Therefore, in a first polish step of Wu, second nitride layer 24A, which is the first layer underlying oxide 34A, is exposed as shown in Fig. 4 of Wu. As further shown in Fig. 4 of Wu, second nitride layer 24A is formed upon and in contact with sacrificial oxide layer 22. In addition, Wu states that "The second nitride layer is removed by H3PO4 because it has high selectivity to nitride, and the sacrificial oxide layer is removed by diluted HF." (Wu -- col. 3, lines 58-60.) Therefore, Wu teaches that the second underlying layer (sacrificial oxide layer 22) is removed by etching. As shown in Fig. 5 of Wu, sacrificial oxide layer 22 is completely removed by etching. Consequently, Wu does not teach that the second underlying layer of sacrificial oxide is polished. As such, Wu does not teach polishing an upper layer of a semiconductor topography to expose a first underlying layer, which is formed upon and in contact with a second underlying layer, etching away remaining portions of the first underlying layer to expose the second underlying layer, and subsequently planarizing the topography, which includes polishing the second underlying layer, as recited in claims 1 and 10. Therefore, Wu does not teach all limitations of claims 1 and 10.

For at least the reasons stated above, Applicants assert that independent claims 1 and 10, as well as claims dependent therefrom, are not anticipated by the cited art. Accordingly, removal of the § 102 rejection of claims 1-4, 6-10, 12-15, 17-19, and 21-24 is respectfully requested.

Section 103 Rejections:

Claim 5 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Wu and further in view of U.S. Patent No. 6,114,216 to Yieh et al. (hereinafter referred to as "Yieh") and U.S. Patent No. 6,348,389 to Chou et al. (hereinafter referred to as "Chou"). Claims 20 and 25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wu. Claim 16 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Wu and further in view Wolf et al. (Silicon Prcessing for the VLSI Era, hereinafter referred to as "Wolf"). As will be set forth in more detail below, the §103(a) rejections of claims 5, 16, 20, and 25 are respectfully traversed.

To establish a *prima facie* obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974), MPEP 2143.03. Obviousness cannot be established by combining or modifying the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion or incentive to do so. *In re Bond,* 910 F. 2d 81, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). The cited art does not teach or suggest all limitations of the currently pending claims, some distinctive limitations of which are set forth in more detail below.

The cited art does not teach or suggest polishing an upper layer of a semiconductor topography to expose a first underlying layer, which is formed upon and in contact with a second underlying layer, etching away remaining portions of the first underlying layer to expose the second underlying layer, and subsequently planarizing the topography, which includes polishing the second underlying layer, as recited in claims 1 and 10. As set forth in more detail above, Wu does not teach all limitations of claims 1 and 10. In addition, Wu does not suggest or provide motivation for all limitations of claims 1 and 10.

In addition, Wu cannot be combined with Yieh, Chou, and/or Wolf to overcome the deficiencies therein. For example, Yieh discloses methods for shallow trench isolation. Yieh states that "the invention relates to a method and apparatus for forming dielectric films over high aspect ratio features at temperatures greater than about 500° C., with the dielectric films having low moisture content and low shrinkage." (Yieh -- col. 2, lines 19-23.) Therefore, Yieh teaches a method and apparatus for depositing dielectric films. However, Yieh does not teach polishing an upper layer of a semiconductor topography to expose a first underlying layer, which is formed upon and in contact with a second underlying layer,

etching away remaining portions of the first underlying layer to expose the second underlying layer, and subsequently planarizing the topography, which includes polishing the second underlying layer, as recited in claims 1 and 10. Consequently, Yieh does not teach all limitations of claims 1 and 10 and cannot be combined with Wu to overcome deficiencies therein.

Chou discloses a method of forming and etching a resist protect oxide layer including end-point etch. For example, Chou states that "the present invention provides a method for forming and etching a resist protect oxide layer, which provides improved etch selectivity to a shallow trench isolation." (Chou -- col. 1, line 66 - col. 2, line 2.) However, Chou does not teach polishing an upper layer of a semiconductor topography to expose a first underlying layer, which is formed upon and in contact with a second underlying layer, etching away remaining portions of the first underlying layer to expose the second underlying layer, and subsequently planarizing the topography, which includes polishing the second underlying layer, as recited in claims 1 and 10. Consequently, Chou does not teach all limitations of claims 1 and 10 and cannot be combined with Wu and/or Yieh to overcome deficiencies therein.

Wolf discloses methods for wet etching of silicon dioxide. For example, Wolf states that "Wet etching of SiO_2 films in microelectronic applications is usually accomplished with various hydrofluoric acid (HF) solutions." (Wolf -- page 532.) However, Wolf does not teach polishing an upper layer of a semiconductor topography to expose a first underlying layer, which is formed upon and in contact with a second underlying layer, etching away remaining portions of the first underlying layer to expose the second underlying layer, and subsequently planarizing the topography, which includes polishing the second underlying layer, as recited in claims 1 and 10. Consequently, Wolf does not teach all limitations of claims 1 and 10 and cannot be combined with Wu, Yieh, and/or Chou to overcome deficiencies therein.

Therefore, none of the cited art, either individually or in any combination thereof, teaches, suggests, or provides motivation for polishing an upper layer of a semiconductor topography to expose a first underlying layer, which is formed upon and in contact with a second underlying layer, etching away remaining portions of the first underlying layer to expose the second underlying layer, and subsequently planarizing the topography, which includes polishing the second underlying layer, as recited in claims 1 and 10. Consequently, the cited art does not teach, suggest, or provide motivation for all limitations of claims 1 and 10.

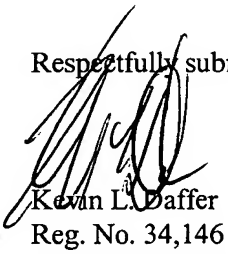
For at least the reasons stated above, claims 1 and 10 are patentably distinct over the cited art. Therefore, claim 5, which depends from claim 1, and claims 16, 20, and 25, which depend from claim 10, are also patentably distinct over the cited art for at least the same reasons. Accordingly, removal of the § 103(a) rejections of claims 5, 16, 20, and 25 is respectfully requested.

CONCLUSION

This response constitutes a complete response to the issues raised in the Office Action mailed August 26, 2003. In view of remarks traversing rejections, Applicants assert that pending claims 1-10 and 12-25 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned attorney earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees, which may be required, or credit any overpayment, to Conley Rose, P.C. Deposit Account No. 03-2769/5298-06500.

Respectfully submitted,



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